NEX806 series

Wide Vcc range quasi-resonant flyback controller

Rev. 1 — 30 September 2024 Product data sheet

1. General description

The NEX806 device series (NEX806xx) are high frequency quasi-resonant PWM controllers implemented with peak current mode control. As the load changes, the NEX806 device automatically switches mode between Quasi-Resonant (QR) mode, Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) mode to maintain a high efficiency across the entire load range. To achieve an ultralow standby power, Burst Mode (BM) is implemented in very light load or no-load condition.

The wide 10 V to 83 V V_{CC} range makes NEX806xx devices suitable for wide output voltage range applications, such as USB PD/PPS which require an output range between 3.3 V to 21 V .

The NEX806xx offers comprehensive protection including output OV/UV, V_{CC} OV/UV, OPP, OCP, line voltage BROWN-IN/OUT, secondary SR short, CS open/short, internal/external OTP, etc.

Furthermore, spread spectrum and smart driving functions can minimize noise and improve EMI performance.

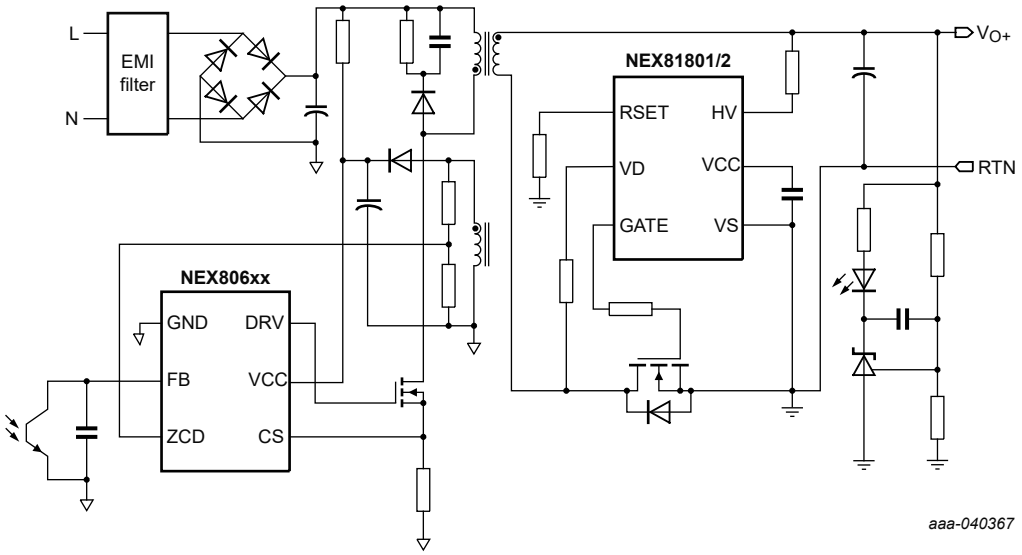
The NEX806xx device series comes in a cost-effective TSOT23-6 package.

2. Features and benefits

- Wide V_{CC} range (10 V-83 V) supports PD/PPS
- Direct GaN driver
- Valley switching operation in QR/DCM/PFM
- Burst Mode with ultra-low operation current in light load and no load
- 130 kHz or 170 kHz maximum frequency options
- Internal Soft Start (SST)
- Output Over Voltage Protection (OVP)
- Spread spectrum for better EMI
- Internal Over Temperature Protection (OTP)
- External OTP by NTC resistor
- V_{CC} Over/Under Voltage Protection (V_{CC} OV/UV)
- Line voltage brown-in /brown-out (BNI/BNO)
- Output Short Circuit Protection (SCP)
- CS Open/Short Protection
- Secondary Rectifier Short Protection (SRSP)
- Overload Protection (OLP)
- Overpower Protection (OPP) to meet LPS
- TSOT23-6 package

3. Applications

- USB PD/QC chargers
- AC/DC adapters for portable devices
- Auxiliary power for industrial and home equipment



4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX80601DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1
NEX80611DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1
NEX80602DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1
NEX80605DA	-40 °C to +125 °C	TSOT23-6FC	Plastic, surface-mounted package; 6 leads	SOT8061-1

5. Marking

Table 2. Marking code

Type number	Marking code
NEX80601DA	NTA
NEX80611DA	NTB
NEX80602DA	NTC
NEX80605DA	NTD

6. Device comparison

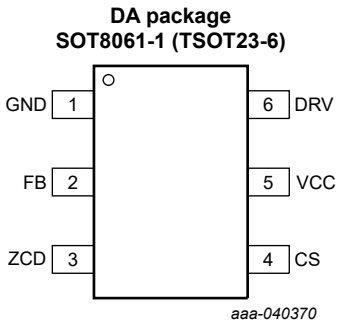
Table 3. Device comparison

Type number	F_{SW_MAX} (kHz)	MOS	I_{out} limited by	Optimized application
NEX80601DA [1]	130	Si/GaN	OPP	65 W/33 W PD
NEX80611DA	130	direct GaN drive	OPP	65 W/33 W PD
NEX80602DA [1]	170	Si/GaN	OPP	65 W/33 W PD
NEX80605DA [1]	130	Si/GaN	OCP	65 W PD

[1] To drive E-mode GaN, external driving circuit is needed.

7. Pinning information

7.1. Pinning



7.2. Pin description

Pin		I/O	Description
Name	Number		
GND	1	PWR	Ground
FB	2	IN	Secondary side voltage feedback pin. Connect to the collector of the opto-coupler.
ZCD	3	IN	Auxiliary voltage sense, brown-in/-out and quasi-resonant valley detection.
CS	4	IN	Current sense pin, connect to the sense resistor of the MOSFET.
VCC	5	PWR	Supply input terminal
DRV	6	OUT	Gate drive output to drive the external MOSFET

8. Product specifications

8.1. Limiting values

Table 4. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.3	100	V
DRV	gate drive voltage		-0.3	V_{DRV_H}	V
CS, FB, ZCD	CS, FB, ZCD voltage		-0.3	5.5	V
T_J	operating junction temperature		-40	T_{SD}	°C
ESD					
V_{ESD}	ESD voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2, all pins except CS	-2000	+2000	V
		HBM: ANSI/ESDA/JEDEC JS-001 class 1C, CS pin only	-1500	+1500	V
		CDM: ANSI/ESDA/JEDEC JS-001 class C2a	-500	+500	V

8.2. Thermal characteristics

Table 5. Thermal characteristics

For more information about thermal metrics consult application note.

Symbol	Parameter	TSOT23	Unit
$R_{\Theta JA}$	junction-to-ambient thermal resistance	127	C/W

8.3. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		10	V_{CC_OVP}	V
CS, ZCD	CS, ZCD voltage		0	5	V
T_J	operating junction temperature		-40	125	°C

8.4. Electrical characteristics

Table 7. Electrical characteristics

Where V_{CC} = 10 V to 90 V; T_J = -40 °C to 125 °C; typical values are measured at V_{CC} = 20 V, T_J = 25 °C (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply (VCC pin)						
V_{CC_ON}	V_{CC} on threshold voltage		-	17	18	V
V_{CC_OFF}	V_{CC} off threshold voltage		-	8.4	-	V
V_{CC_HOLD}	V_{CC} hold threshold votlage		-	9	9.4	V
V_{CC_OVP}	V_{CC} OVP threshold votlage		83.5	89	93	V
V_{CC_DIS}	V_{CC} discharge threshold votlage		-	94	99	V
$V_{CC\_DIS\_HYS}$	V_{CC} discharge threshold hysteresis votlage		-	5	-	V
I_{DIS}	V_{CC} discharge current		-	5	-	mA
$I_{STARTUP}$	V_{CC} startup current		-	5	8	µA
I_{NORMAL}	V_{CC} normal operating current	NEX80601, NEX80605; F_{SW} = 130 kHz, V_{CC} = 20 V, 1 nF at DRV pin	-	1.9	2.66	mA
		NEX80611; F_{SW} = 130 kHz, V_{CC} = 20 V, 1 nF at DRV pin	-	1.35	1.89	mA
		NEX80602; F_{SW} = 170 kHz, V_{CC} = 20 V, 1 nF at DRV pin	-	2.3	3.22	mA
I_{BURST}	V_{CC} current in burst mode			270	350	µA
Feedback input (FB pin)						
V_{FB_OPEN}	FB pin open-circuit voltage		-	5	-	V
R_{FB}	FB internal pull-up resistor		-	28	-	kΩ
$V_{FB\_BURST\_OFF}$	FB voltage when DRV pulse is skipped		-	0.3	-	V
$V_{FB\_BURST\_ON}$	FB voltage when DRV pulse is resumed		-	0.4	-	V
V_{FB_OLP}	overload protection threshold voltage		-	3.5	-	V
t_{D_OLP}	overload protection deglitch time		-	50	-	ms
K_{FB}	divider ratio from FB to CS		-	5	-	V/V
t_{SS}	soft start time	0 to 0.4 V V_{CS}	-	4.3	-	ms
Current sense input (CS pin)						
t_{LEB_PWM}	leading edge blanking for PWM comparator		-	320	-	ns
$V_{CS\_PWM\_MAX}$	maximum current limit threshold for PWM comparator		0.365	0.4	0.43	V
t_{LEB_OCF}	leading edge blanking for OC fault protection		-	90	-	ns
V_{CS_OCF}	secondary rectifier (SR) short circuit fault protection		0.61	0.65	0.7	V
t_{D_OCF}	SR short-circuit fault deglitch cycles		-	3	-	cycles
V_{CS_SHORT}	CS pin short detection threshold		-	0.04	-	V
$t_{BLK\_CS\_SHORT}$	CS pin short detection blanking time	I_{line} = 90 µA	-	3	-	µs
$t_{D\_CS\_SHORT}$	CS pin short fault deglitch cycles		-	3	-	cycles

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Zero current detection (ZCD pin)						
I_{ZCD_VALLEY}	Valley detection threshold		-	9	-	µA
t_{W_VALLEY}	Valley window time		-	2	-	µs
I_{BNI}	Brown-in detection threshold	T_J = 25 °C	-	91	96	µA
I_{BNO}	Brown-out detection threshold [1]		79	85	91	µA
t_{D_BNO}	Brown-out deglitch time		-	50	-	ms
V_{ZCD_OVP}	ZCD OVP threshold		3.3	3.6	3.8	V
$t_{D\_ZCD\_OVP}$	ZCD OVP deglitch time		-	7	-	cycles
V_{ZCD_SCP}	Output short-circuits protection threshold		-	0.3	-	V
$t_{D\_ZCD\_SCP}$	Output short-circuits protection deglitch time		-	7	-	cycles
t_{BLK_UVP}	UVP/SCP blanking time during softstart		-	20	-	ms
Gate Drive (DRV pin)						
V_{DRV_L}	DRV low level		-	-	0.2	V
V_{DRV_H}	DRV high level	NEX80601/NEX80602/ NEX80605; V_{CC} = 12 V	8	-	-	V
	DRV high level clamp voltage	NEX80601/ NEX80602/ NEX80605; V_{CC} ≥ 15 V	-	11.5	-	V
	DRV high level clamp voltage	NEX80611; V_{CC} = 12 V	-	5.8	6.9	V
t_r	DRV rising time	C_{load}= 1 nF	-	350	-	ns
t_f	DRV falling time	C_{load}= 1 nF	-	30	-	ns
Control law						
F_{MAX}	maximum switching frequency	NEX80601/NEX80611/ NEX80605	120	130	140	kHz
		NEX80602	155	170	185	kHz
F_{MIN}	minimum switching frequency		20	25	30	kHz
Over temperature protection						
T_{SD}	internal thermal shutdown threshold		-	155	-	°C
T_{SD_HYS}	internal thermal shutdown hysteresis		-	30	-	°C
V_{CS_OTP}	external OTP trigger voltage		-	V_{ZCD}/7	-	V
T_{D_OTP}	external OTP deglitch time		-	1.5	-	ms

[1] Guaranteed by design.

8.5. Typical characteristics

Table 8. Typical characteristics

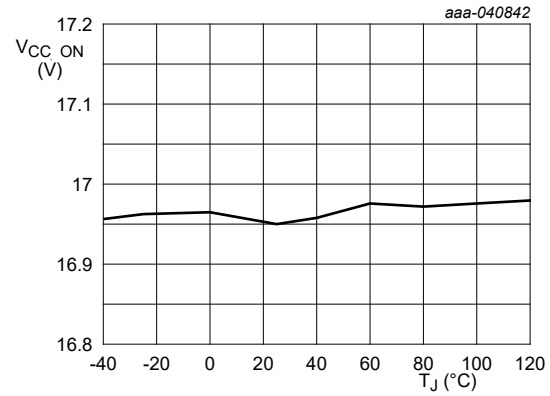


Fig. 1. V_{CC_ON} vs. junction temperature

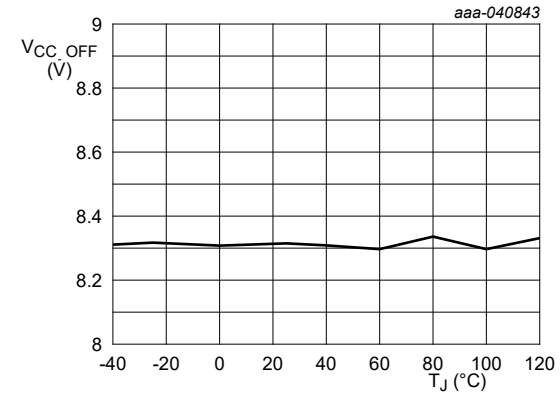


Fig. 2. V_{CC_OFF} vs. junction temperature

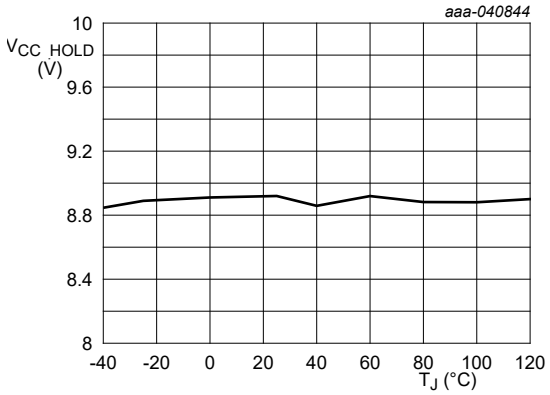


Fig. 3. V_{CC_HOLD} vs. junction temperature

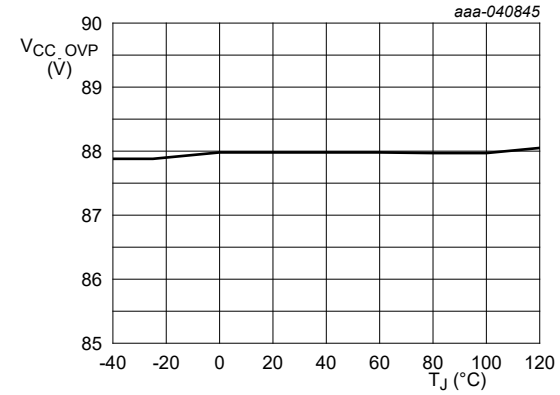
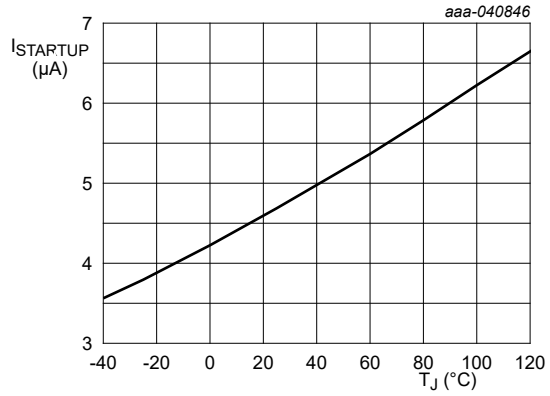
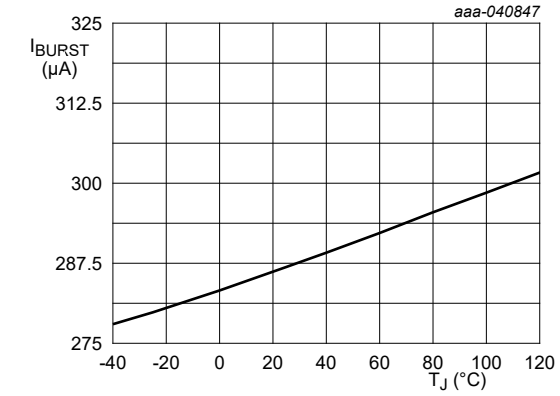


Fig. 4. V_{CC_OVP} vs. junction temperature



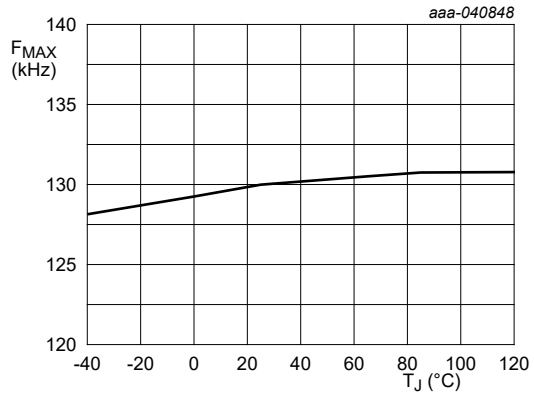
V_{CC} = 16 V

Fig. 5. $I_{STARTUP}$ vs. junction temperature



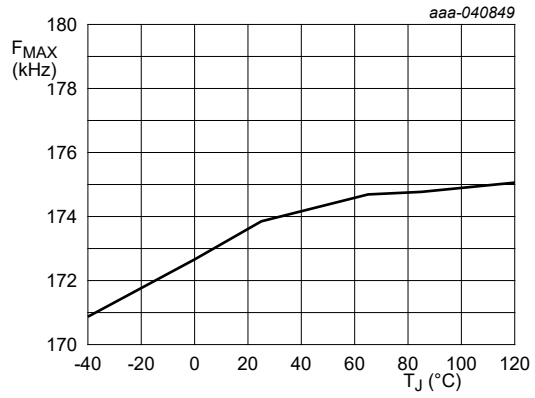
V_{CC} = 20 V

Fig. 6. I_{BURST} vs. junction temperature



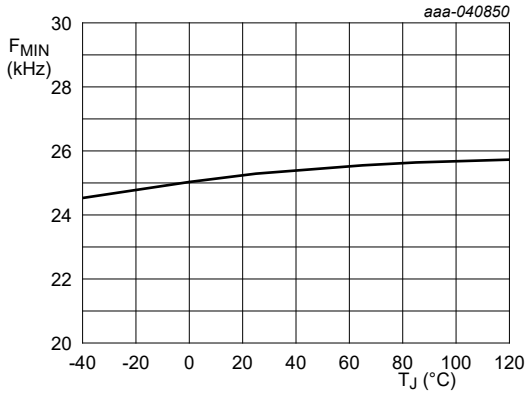
For NEX80601, NEX80611, NEX80605;
V_{CC} = 20 V

Fig. 7. F_{MAX} vs. junction tempertaure



For NEX80602;
V_{CC} = 20 V

Fig. 8. F_{MAX} vs. junction tempertaure



V_{CC} = 20 V

Fig. 9. F_{MIN} vs. junction temperature

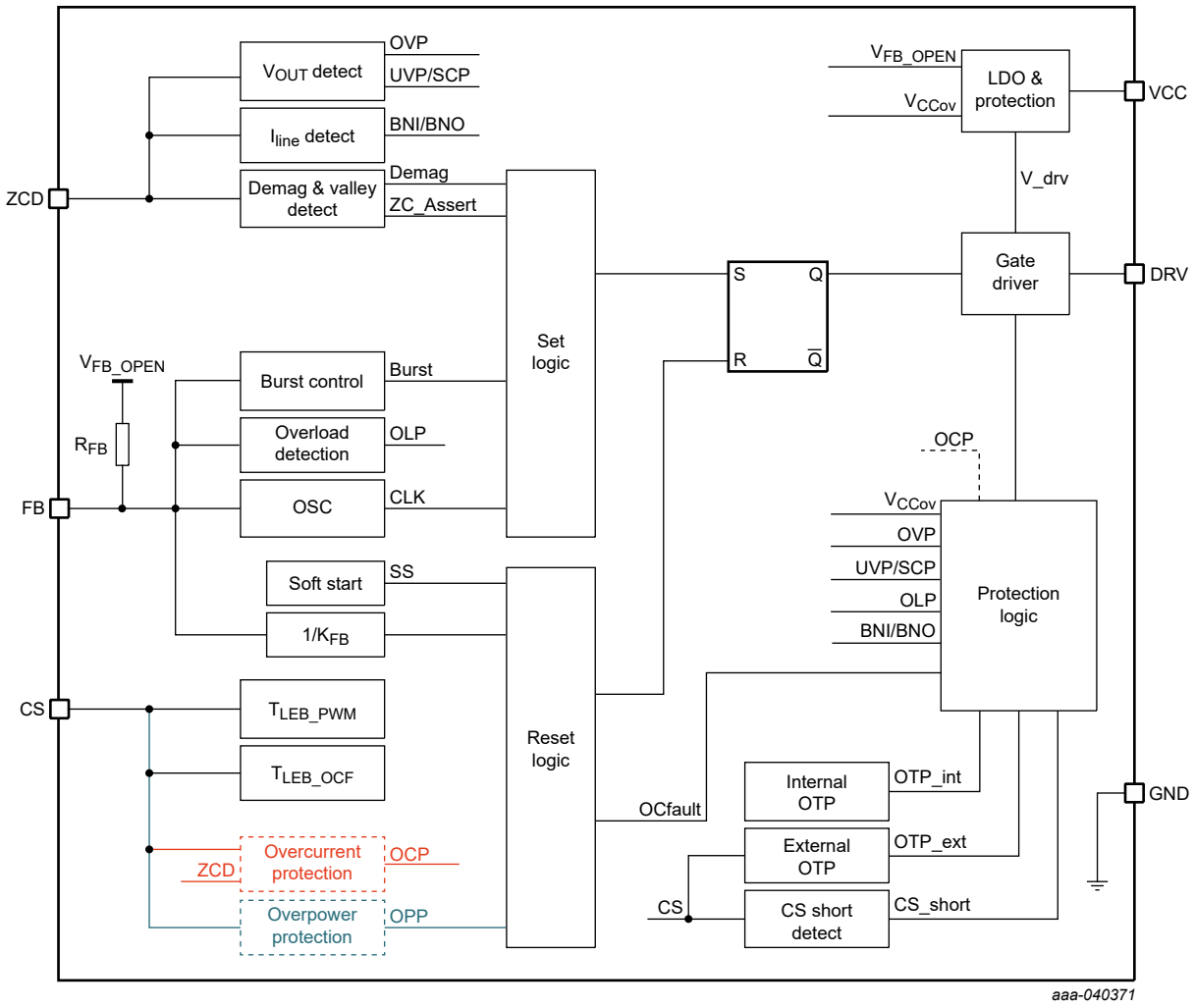
9. Detailed Description

9.1. Overview

The NEX806xx is a high frequency Quasi-Resonant (QR) PWM controllers with peak current mode control. Under conditions of low input line voltage and heavy load, the NEX806xx works in Quasi-Resonant (QR) Mode with valley switching to reduce the switching loss. As the input voltage increases, or the load current decreases, the devices gradually enter Discontinuous Conduction Mode (DCM) with the frequency clamped at the maximum limitation. As the load current further decreases, it enters Pulse Frequency Modulation (PFM) mode with frequency foldback to maintain a high efficiency across the entire load range. To achieve an ultralow standby power, Burst Mode (BM) is implemented in very light load or no-load condition, while the minimum switching frequency is fixed at 25 kHz to avoid audible noise.

9.2. Functional block diagram

The functional block diagram for the NEX806xx series of products is shown in Figure 1.



NEX80601/80611/80602 do not have OCP block. NEX80605 does not have OPP block.

Fig. 10. Function block diagram

9.3. Feature description

9.3.1. Startup

The NEX806xx devices are enabled when V_{CC} voltage is higher than turn-on threshold V_{CC_ON}, and disabled when it drops below turn-off threshold, V_{CC_OFF}. The voltage dips during startup; a hysteresis is built in to avoid shutdown during this process. As the AC input voltage is supplied, the voltage across the input bulk capacitor will charge up V_{CC} cap through the startup resistor R_{START} as shown in Fig. 11. Before being enabled, the VCC pin consumes only $I_{STARTUP}$ which is typically 5 µA. Thus, a relatively larger value can be chosen for R_{START} to reduce the power consumption. However, too large of a resistance for R_{START} will increase the startup time. Nexperia recommends using two 1.5 MΩ resistors with 1206 package in series for R_{START}.

Once V_{CC} voltage is higher than V_{CC_ON} threshold, the NEX806xx is enabled and the DRV pulse is generated to drive external MOS. The current consumption at the VCC pin will increase to I_{NORMAL}, which is much higher than the current from startup resistor. Then the V_{CC} voltage decreases. It is important that the auxiliary winding voltage increases enough to take over and maintain the V_{CC} voltage in the normal range before it drops below V_{CC_OFF}. The capacitance of the V_{CC} capacitor should be carefully sized to meet this requirement. A 4.7 µF electrolytic capacitor is normally used here. The timing sequence of startup is shown in Fig. 12

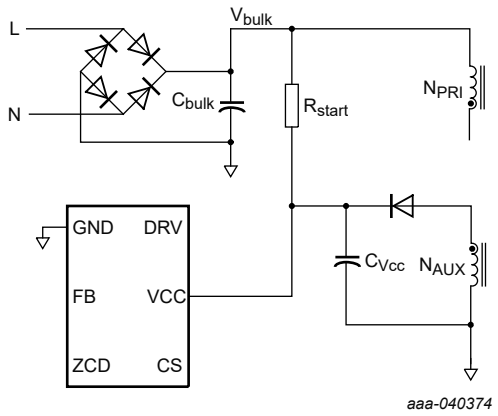


Fig. 11. Typical startup circuit

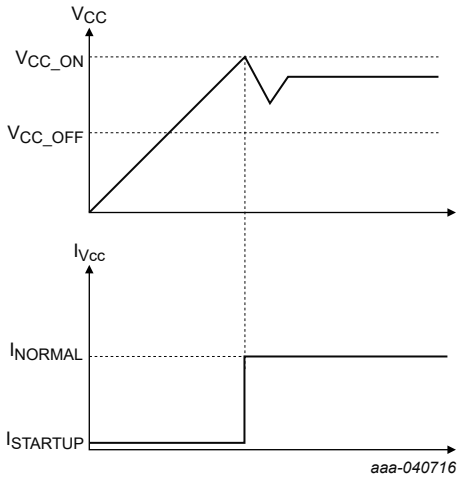


Fig. 12. Timing sequence of startup

9.3.2. Brown-in/brown-out

Besides the detection of V_{CC} voltage, the input line voltage is also checked before the soft start is initiated. When the primary MOS is turned on, the induced auxiliary winding voltage is negative, a current flowing out from ZCD pin is generated. See Fig. 13 for reference.

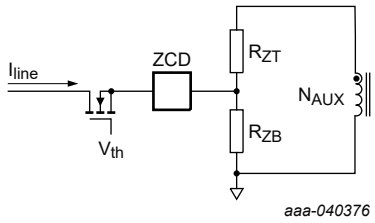


Fig. 13. Resistor divider at ZCD

Since the ZCD voltage is clamped at ~0 V by internal circuit, this current is proportional to input voltage and can be calculated as shown Equation 1:

$$I_{line} = \frac{V_{BULK} \times N_{AUX}}{N_{PRI} \times R_{ZT}} \quad (1)$$

where N_{PRI} and N_{AUX} are the number of turns of primary winding and auxiliary winding respectively, and R_{ZT} is the top side resistor of the divider from auxiliary winding to ZCD pin.

Each time V_{CC} is higher than V_{CC_ON}, the NEX806xx will send out several narrow pulses to turn on the primary MOS, then detect I_{line}. If $I_{line} > I_{BNI}$, the brown-in threshold current, the NEX806xx will initiate the soft start process; if $I_{line} \leq I_{BNI}$ NEX806xx will restart.

During the normal working period, I_{line} is always checked when the primary MOS is turned on. If I_{line} is below I_{BNO}, the brown-out threshold current, for a continuous time longer than t_{D_BNO} (~50 ms), NEX806xx will restart. The timing sequence of the brown-out is shown in Fig. 14.

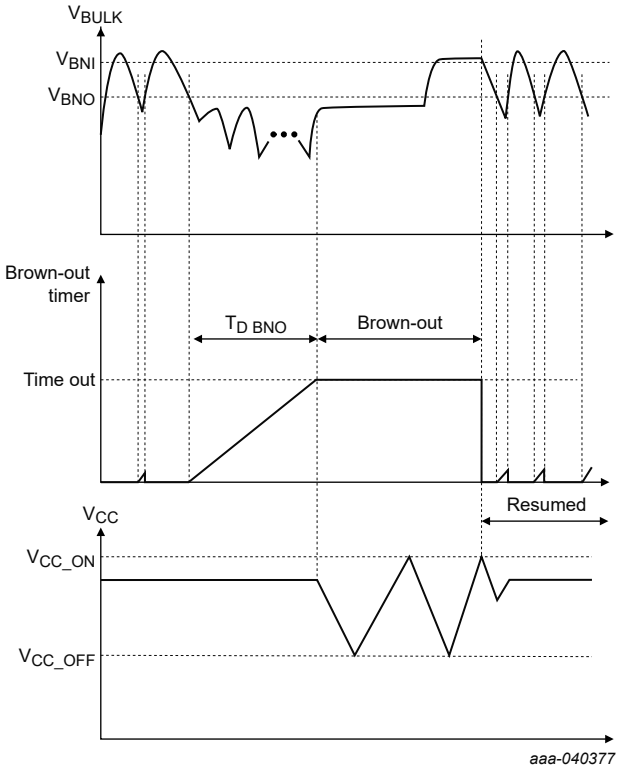


Fig. 14. Timing sequence of brown-out

9.3.3. V_{CC} holding mode

In very light load conditions, the NEX806xx may stay in the burst off-state for a long time when the output voltage is higher than the target. V_{CC} voltage may drop below V_{CC_OFF} since there is no driving pulse. This triggers the restart. To avoid this, the NEX806xx will send out the driving pulse once V_{CC} is below V_{CC_HOLD} , which is slightly higher than V_{CC_OFF}. The NEX806xx will stop the driving pulse when V_{CC} returns to V_{CC_HOLD} plus hysteresis; this is called V_{CC} Holding Mode.

For wide output voltage range applications, the turn ratio of auxiliary winding and secondary winding should be properly selected to make sure the V_{CC} Holding Mode will not be triggered at the minimum output voltage condition, since V_{CC} Holding Mode will override the normal output voltage regulation.

9.3.4. Current sense and peak current control

To implement peak current mode control, R_S, the sense resistor, is connected between the source of the primary MOS and GND to sense the primary current. The sense voltage across R_S is feedback to the CS pin, which is compared to the peak-control voltage to determine the duty cycle of the primary MOS. The peak-control voltage is generated from FB voltage divided by K_{FB} (typically 5), where the FB voltage is commanded by the voltage control loop to regulate the output voltage, see Fig. 15. The maximum peak-control voltage is clamped at $V_{CS\_PWM\_MAX}$ (~400 mV) internally. Then the maximum transformer primary current can be obtained using Equation 2:

$$I_{\mathrm{Peak\_max}} = \frac{V_{\mathrm{CS\_PWM\_MAX}}}{R_S} \quad (2)$$

Due to the parasitic capacitance of the primary MOS and transformer, a large voltage spike often appears on the CS pin at the turn-on moment. To prevent this spike from falsely triggering the current sense comparator, a leading-edge-blanking (LEB) time t_{LEB_PWM} (~320 ns) is included in the input of CS pin. If this internal LEB time is not long enough, an external R-C filter can be added between the sense resistor and CS pin.

9.3.5. Soft start

The soft start process is initiated when V_{CC} is higher than V_{CC_ON} threshold, and the input voltage is higher than the brown-in threshold. During this period, the peak voltage on the CS pin is limited by the SS signals, which ramps up from 0 mV to 400 mV within t_{SS}, which is typically 4.3 ms. This means the primary peak current increases slowly in the soft start period, the output voltage can ramp up without overshoot, and the voltage/current stress on the secondary rectifier is minimized.

9.3.6. Voltage control loop

The output voltage is sensed by a resistor divider and provides feedback to an error amplifier (usually TL431 is used). The output of the error amplifier drives an opto-coupler to generate the command voltage at the FB pin. The FB voltage, combined with the internal current loop, controls the output voltage. The typical circuit of voltage control loop is shown in Fig. 15.

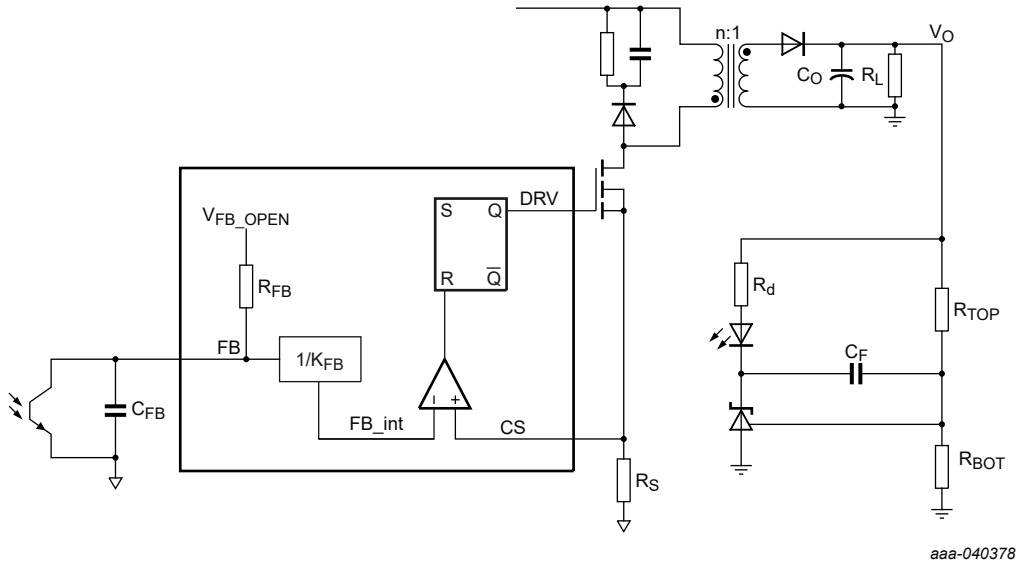


Fig. 15. Typical circuit of voltage control

9.3.7. QR/DCM/PFM operation

NEX806xx is a high frequency Quasi-Resonant (QR) PWM controller implemented with peak current mode control. As the load changes, it automatically switches the working mode between QR Mode, Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) mode with valley switching.To maintain a high efficiency across the entire load range, turning on the primary MOS is always gated by CLK signal, which is the clamping frequency commanded by FB voltage.

Under heavy load and low line conditions, FB is high, which means the primary peak current and clamp frequency is high. Since a longer time is needed for demagnetization, the clamping frequency signal (CLK) arrives before demagnetization. The power MOS will not be turned on until demagnetization and the following valley moment is detected (see Fig. 16 and Section 9.3.10).The power MOS turns on at the first valley after demagnetization, and the converter works in QR mode.

As load decreases, or line voltage increases, FB voltage will decrease, which means the primary peak current and clamp frequency decreases. Demagnetization can be finished before the clock signal. In this condition, the power MOS will not be turned on until the clock signal and the following valley moment are detected. In this situation, if the clamp frequency is still at the maximum frequency, the converter works in DCM; if the clamp frequency is below the maximum, the converter works in PFM.

If the load continues to decrease, the clamp frequency further decreases as FB voltage decreases. The ringing amplitude at auxiliary winding may be damped too small for a valley moment to be detected after clock arrives. In this case, once the t_{W_VALLEY} time expires after CLK, the primary MOS will be forced on.

9.3.8. Burst mode control

As the load decreases, FB voltage will decrease to regulate the output voltage. As a result, the peak-control voltage (equal to the peak voltage of CS) decreases and is finally clamped at its minimum limit (typically ~90 mV). Meanwhile, the switching frequency also decreases and is clamped at F_{MIN} (typically 25 kHz) to avoid audible noise. If the load decreases further, FB voltage will drop below the $V_{FB\_BURST\_OFF}$ threshold (typically 0.3 V) and DRV pulse is disabled. In this burst-off period, V_{CC} current drops to I_{BURST} (typically 270 µA). At this moment, since no power is being delivered to the output anymore, the output voltage begins decrease. The voltage control loop will increase FB voltage gradually. Once FB voltage is higher than $V_{FB\_BURST\_ON}$ threshold (typically 0.4 V), the DRV pulse is resumed. Using this method of burst mode control improves the light load efficiency significantly.

9.3.9. ZCD voltage detection

During the flyback period, the information of output voltage can be derived by sampling ZCD voltage as shown in Fig. 16.

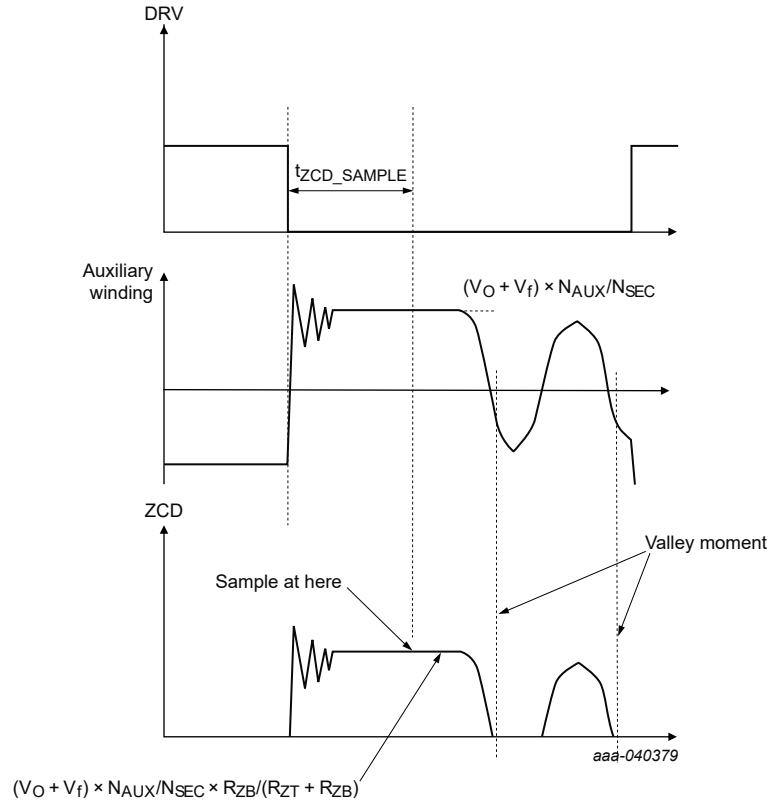


Fig. 16. ZCD voltage detection and valley detection

The output voltage OVP and UVP/SCP protection are implemented by comparing the sampled ZCD voltage with different threshold voltage.

The output voltage OVP protection is triggered if the sampled ZCD voltage is higher than OVP threshold for seven consecutive cycles.

The output voltage short-circuit protection (SCP) is triggered if the sampled ZCD voltage is lower than SCP threshold V_{ZCD_SCP} (0.3 V typically) for seven consecutive cycles.

Since the output voltage need time to setup, the UVP/SCP protection is disabled for a t_{BLK_UVP} blanking time during soft start.

Due to the leakage inductance of transformer, there is large ringing waveform at ZCD pin at the beginning of flyback period. To avoid sampling at this ringing moment, a blanking time is added after the going-low of DRV signal. ZCD sampling is not allowed until this blanking window expires.

9.3.10. Valley switching

During QR/DCM/PFM mode, once the magnetizing current decreases to zero, the primary inductor begins oscillating with the parasitic capacitor of the primary MOS. It is ideal to turn on the primary MOS at the valley moment of oscillation to minimize the switching loss. As shown in Fig. 16, when the auxiliary winding voltage becomes negative, ZCD pin is clamped at ~0 V internally, and the current flowing out of ZCD pin is detected. Once the current is larger than I_{ZCD_VALLEY} (~9 µA), that moment is identified as a valley moment. Several valley moments may be identified before CLK signal arrives. The valley moment just behind CLK is chosen as the moment to turn on the primary MOS.

9.3.11. Oscillator frequency

The NEX806xx is specially designed for wide output voltage range applications. To optimize the efficiency of each output voltage condition, the maximum switching frequency is adjusted according to the target output voltage, as derived by ZCD detection. Different frequency-vs-FB curves are used for different output voltage conditions.

As FB voltage decreases, the clamp frequency CLK will decrease until it arrives the minimum limit F_{MIN} (typically 25 kHz, to avoid audible noise), thus a relatively high efficiency is achieved in the whole load range.

To optimize the EMI performance, spread-spectrum function is implemented.

9.3.12. Driver

For NEX80601/80602/80605, which are designed to drive Si MOS or D-mode GaN MOS directly, the typical high voltage levels on the DRV pin is clamped by an internal voltage clamp (typically 11.5 V). For a normal 12 V V_{CC} supply, the DRV amplitude is guaranteed to be higher than 8 V. This gives enough voltage to fully turn on the high-voltage MOSFETs, while providing an adequate margin to avoid overvoltage damage of the gate, since most high-voltage MOSFETs have a maximum gate voltage rating of 20 V. By adding external driving and clamping circuits, NEX80601/80602/80605 can also drive e-mode GaN MOS.

For NEX80611 ,which is designed to drive e-mode GaN MOS directly, the typical high voltage level on the DRV pin is 5.8 V, with a maximum limit of 6.9 V.

9.3.13. Restart

When the restart process is triggered, the DRV pulse is stopped. Then V_{CC} voltage declines, since there is no supply from auxiliary winding. Once V_{CC} drops below the V_{CC_OFF} threshold, the device is disabled and the V_{CC} current consumption drops to $I_{STARTUP}$ (typically 5 µA), the V_{CC} capacitor will be charged up by the startup resistor. When V_{CC} voltage rises above V_{CC_ON}, a soft start process is initiated if the line voltage meets the brown-in requirement.

9.3.14. Overload protection (OLP)

If the load current is higher than the maximum allowed output current limit, the output voltage will decrease, and FB voltage will increase. If FB voltage is higher than V_{FB_OLP} (typically 3.5 V) for a period t_{D_OLP}, overload protection is triggered, and the device will restart.

9.3.15. Overpower protection (OPP)

To meet the Limited Power Source (LPS) requirements, the maximum output current of the power supply should be less than 8A, and the output power should not exceed 100 W under any condition. However, with a fixed primary peak current limit, the output current and output power will increase as input line voltage increase, so LPS is likely to be violated.

The NEX80601/80611/80602 devices use the input line voltage information to compensate the primary peak current limit. The higher the input line voltage is, the lower the primary peak current limit is, thus a relatively constant output current/ power limit can be achieved. A resistor, R_{SERIES}, between the current sense resistor and CS pin can be used to fine tune the primary peak current limit, see Fig. 17. The resistance of R_{SERIES} is suggested to be less than 1 kΩ. If the load current is higher than the output current limit, the output voltage will drop, FB voltage will increase. If FB voltage is higher than V_{FB_OLP} (typically 3.5 V) for a period t_{D_OLP}, overload protection is triggered, and the device will restart. This limits the maximum output power.

9.3.16. Over current protection (OCP)

To better meet LPS requirements, NEX80605 uses the OCP method. By detecting the peak primary current, as well as the demagnetization duty, NEX80605 calculates the output current of the flyback circuit. If the calculated value is higher than the target current limit for a preset period, the OCP is triggered, and the device will restart.

9.3.17. Secondary rectifier short-circuit protection (SRSP)

In case the secondary rectifier is short-circuited, the primary MOS current increases very fast at the turn on moment, an immediate protection is needed here. A shorter blanking time t_{LEB_OCF} (~90 ns) is implemented to address this problem. Each time the primary MOS is turned on, once the blanking time t_{LEB_OCF} expires, the primary current is sampled and feedback to CS pin. If it's higher than the SR short-circuit fault protection threshold V_{CS_OCF} (~650 mV), the primary MOS is turned off immediately. If this event happens for 3 consecutive cycles, the device will restart.

9.3.18. V_{cc} overvoltage protection (V_{CC} OVP)

Once V_{CC} voltage is higher than threshold V_{CC_OVP} (typically 89 V), V_{CC} OVP is triggered, and the device restarts. In some abnormal conditions, for example, when the startup resistance is too low, V_{CC} voltage is pulled up even though the device is in restart condition. If V_{CC} voltage is pulled higher than V_{CC_DIS} threshold (typically 94 V), a sink current $I_{DISCHARGE}$ (5 mA typical) will discharge V_{CC} voltage until it is below 89 V. This prevents the VCC pin from being damaged by overvoltage in abnormal conditions.

9.3.19. Over temperature protection (OTP)

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. Once the T_J exceeds the thermal shutdown threshold T_{SD} (155 °C typical), the device shutdown and DRV pulse stops, the device temperature decreases. When T_J is below 125 °C, the device will restart.

Besides the internal OTP, the NEX806xx also implements an external OTP function. By adding an NTC resistor at the key component of the power supply, that component can be protected from over temperature damage. This method is shown in Fig. 17.

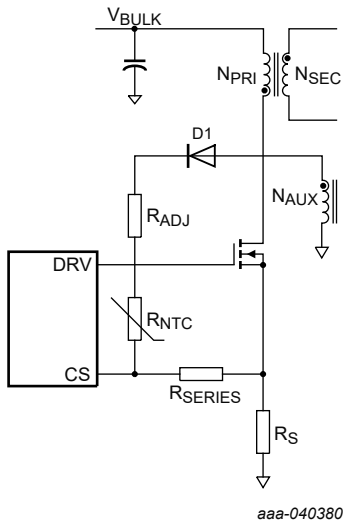


Fig. 17. Typical application circuit of external OTP

When the primary MOS is turned off, the auxiliary winding voltage is feedback to the CS pin by resistor divider. Under normal conditions, the NTC resistor R_{NTC} has a large resistance. This results in a very low voltage at the CS pin. For abnormal conditions, the NTC resistor temperature increases much higher due to the key component under protection, so the resistance of R_{NTC} decreases significantly, which leads to an increase in the divided voltage at the CS pin. If the voltage on the CS pin is higher than threshold V_{CS_OTP} for t_{D_OTP} (typically 1.5 ms), the external OTP is triggered, the device stops DRV pulse and restarts.

The resistance of R_{NTC} that triggering external OTP can be calculated in Equation 3:

$$R_{NTC(OTP)} = R_{series} \times \left(\frac{\left(N_{AUX} / N_{SEC} \right) \times V_O - V_d}{V_{CS\_OTP}} - 1 \right) - R_{ADJ} \quad (3)$$

where N_{AUX} and N_{SEC} are the turn numbers of auxiliary and secondary windings respectively. Vd is the forward voltage of D1. The resistor R_{ADJ} is used to fine tune the external OTP temperature at target threshold.

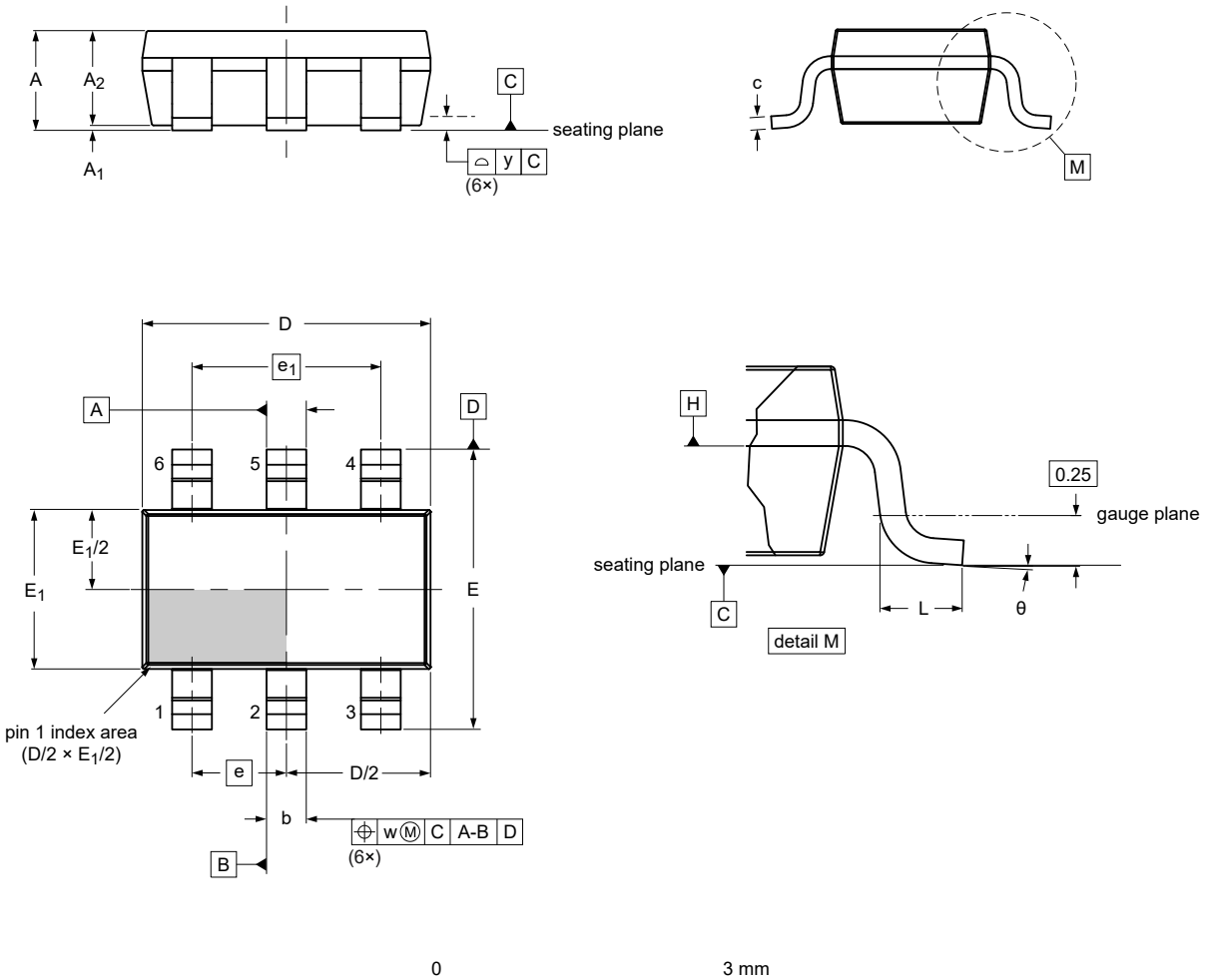
For wide output voltage range applications, to get a relatively constant external OTP temperature for different output voltage condition, the NEX806xx automatically adjusts the OTP threshold V_{CS_OTP} to be proportional to the output voltage.

9.3.20. CS pin short protection

In case the CS pin is shorted to GND, or the sense resistor R_S is shorted, the primary current will lose control. This is dangerous and must be prevented. Each time the primary MOS is turned on, a blanking timer $t_{BLK\_CS\_SHORT}$ starts. When it expires, if the MOS is not turned off yet, the CS pin voltage will be compared with V_{CS_SHORT} threshold (typcically 40 mV). If the CS pin voltage lower than threshold, this indicates a CS short failure, and the primary MOS will be turned off immediately. If this event happens for three consecutive cycles, the NEX806xx will restart.

10. Package outline

Plastic, surface-mounted package (TSOT23-6); 6 leads **SOT8061-1**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	E	E_1	e	e_1	L	y	w	θ
mm	max	1.10	0.10	1.00	0.50	0.20	3.05	3.00	1.75	0.95 BSC	1.90 BSC	0.60	0.10	0.20	8°
	nom						2.90	2.80	1.60						
	min		0.00	0.70	0.30	0.08	2.75	2.60	1.45			0.30			0°

Note
Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.25 mm per end.
Dimension E_1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0. 25 mm per side.
D and E_1 dimensions are determined at datum H.

sot8061-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8061-1		MO-193				~~24-09-04~~ 24-09-16

Fig. 18. Package outline SOT8061-1 (TSOT23-6)

11. Abbreviations

Table 9. Abbreviations

Acronym	Description
AC	Alternating Current
BM	Burst Mode
CCM	Continuous Conduction Mode
CDM	Charged Device Model
DC	Direct Current
DCM	Discontinuous Conduction Mode
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
HBM	Human Body Model
HV	High Voltage
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LPS	Limited Power Source
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OCP	OverCurrent Protection
OLP	OverLoad Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PFM	Pulse Frequency Modulation
QR	Quasi-Resonant
SRSP	Synchronous Rectifier Short Protection
USB	Universal Serial Bus
UVLO	Under-Voltage LockOut

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX806_series v.1	20240930	Product data sheet	-	-

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
Date of release: 30 September 2024

Contents

1. General description....1
2. Features and benefits....1
3. Applications....1
4. Ordering information....2
5. Marking....2
6. Device comparison....2
7. Pinning information....2
7.1. Pinning....2
7.2. Pin description....3
8. Product specifications....3
8.1. Limiting values....3
8.2. Thermal characteristics....3
8.3. Recommended operating conditions....3
8.4. Electrical characteristics....4
8.5. Typical characteristics....6
9. Detailed Description....8
9.1. Overview....8
9.2. Functional block diagram....8
9.3. Feature description....9
9.3.1. Startup....9
9.3.2. Brown-in/brown-out....10
9.3.3. V_{CC} holding mode....11
9.3.4. Current sense and peak current control....11
9.3.5. Soft start....11
9.3.6. Voltage control loop....12
9.3.7. QR/DCM/PFM operation....12
9.3.8. Burst mode control....12
9.3.9. ZCD voltage detection....13
9.3.10. Valley switching....13
9.3.11. Oscillator frequency....14
9.3.12. Driver....14
9.3.13. Restart....14
9.3.14. Overload protection (OLP)....14
9.3.15. Overpower protection (OPP)....14
9.3.16. Over current protection (OCP)....14
9.3.17. Secondary rectifier short-circuit protection (SRSP)....15
9.3.18. V_{cc} overvoltage protection (V_{CC} OVP)....15
9.3.19. Over temperature protection (OTP)....15
9.3.20. CS pin short protection....16
10. Package outline....17
11. Abbreviations....18
12. Revision history....19
13. Legal information....20